Tutorial 6 - SS2017
Communication Systems and Protocols

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Task 1: CAN Bus

Since CAN uses CSMA/CA as arbitration scheme every participant compares the actual bus level with the signal transmitted by itself. Because of that it is important for every participant to be able to evaluate the actual state on the bus before begin of a new bit. Here beside the signal runtime on the bus also the required processing time of the participant itself plays a role.

As given in Figure 1.1, this includes the processing time t_{CAN} of the CAN controller, the times t_{Rx} and t_{Tx} which are needed inside the transceiver for reception and transmission as well as the runtime t_{Bus} on the bus.

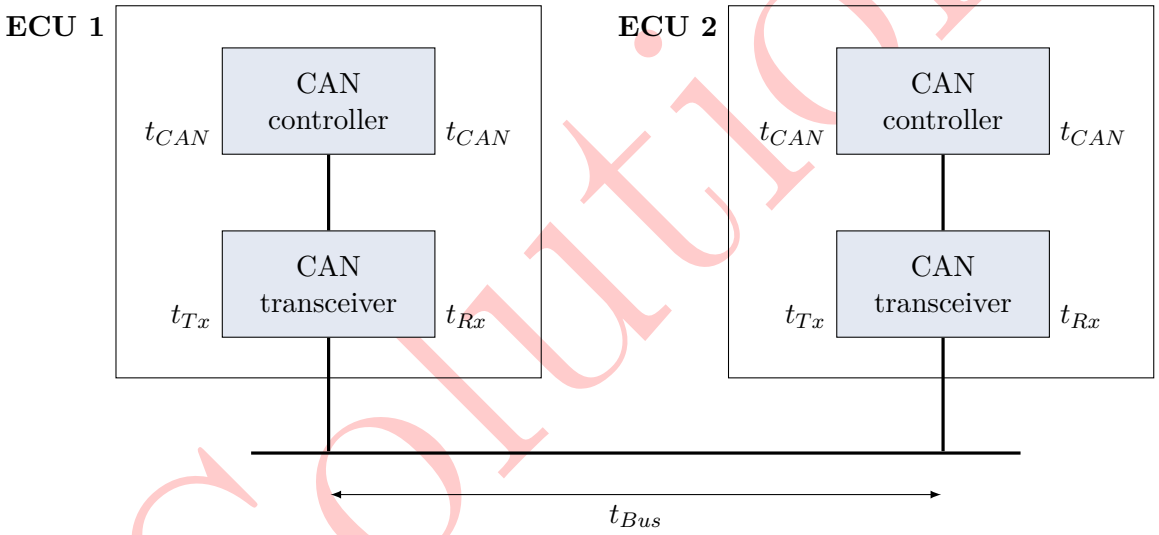


Figure 1.1: CAN bus

A) What is the interrelation between the maximum bus length and the bit transmission rate for CAN? Neglect the processing time inside the ECUs for this question

1

Condition of simultaneity has to be fulfilled.
T_{Bit}: Duration for transmission of one bit
T_{Prop}: Signal runtime on the bus

Interrelation: $T_{Bit} >> T_{Prop}$

$\Rightarrow \frac{1}{TR} >> \frac{l}{v}$
TRTransmission rate, l Maximum bus length, v Velocity of propagation

B) Based on the previous question, specify the maximum bus length for a speed of propagation of $v = 2.3 \cdot 10^8 m/s$ and for the transmission rates of $10 kbit/s$ and $1 Mbit/s$ respectively. **1**

First node to start an arbitration has to wait at least 2 times the duration for propagation of a signal on the bus until it gets a valid signal on the bus:

- One node starts arbitration. After 1x T_{Prop} the signal reaches the node at the end of the bus.
- Now this node knows that a new arbitration has started and sends out its own ID bit.
- The signals reaches the first node after another T_{Prop}. Now we have a stable value on the bus, 2x T_{Prop} after the first node started transmission.

$T_{Bit} \geq 2 \cdot T_{Prop} \Rightarrow l \leq \frac{v}{2 \cdot TR}$
For $10 kbits/s$: $l \leq \frac{2.3 \cdot 10^8 m/s}{2 \cdot 10 kbit/s} \Rightarrow l \leq 11500m$
For $1 Mbit/s$: $\Rightarrow l \leq 115m$

C) Now also consider the delays inside the ECUs. Which data transmission rate can be set as a maximum if the bus length between the two controllers that have furthest distance amounts to 300 meters? The detection of the bus state shall be accomplished after 80 percent of the bit time at latest (assume: $t_{CAN} = 75nsec$, $t_{Rx} = t_{Tx} = 25nsec$, $v_{Bus} = 0,2m/nsec$). **2**

Maximum transmission rate

Delay inside the participants:
$t_{TN} = 2 \cdot t_{CAN} + t_{Tx} + t_{Rx} = 2 \cdot 75ns + 2 \cdot 25ns = 200ns$
Delay on the bus:
$t_{Bus} = \frac{l_{Bus}}{v_{Bus}} = \frac{300m}{0.2m/ns} = 1500ns = 1.5\mu s$
Minimum bit duration:
$t_{Bit} \geq 2 \cdot (t_{TN} + t_{Bus}) = 2(0.2\mu s + 1.5\mu s) = 3.4\mu s$
Maximum transmission speed:
$S = \frac{1}{t_{Bit} * 0.8} = \frac{1}{3.4\mu s \cdot 0.8} = 368 Kbit/s$

2

Task 2: Universal Serial Bus (USB)

A) Consider an USB 1.1 device in reset state. Calculate the current on the bus. Neglect the energy needs of the device itself. Use the circuit in Figure 2.1 as orientation. 1

The current flow on the bus is determined by the series connection of R_1 and R_2:

$$R_1 + R_2 = 15k\Omega + 1,5k\Omega = 16.5k\Omega$$

$$I = \frac{U}{R} = \frac{3.3V}{16.5k\Omega} = 200\mu A$$

As a comparison: Maximum current consumption in standby in accordance with the specification: $500\mu A$.

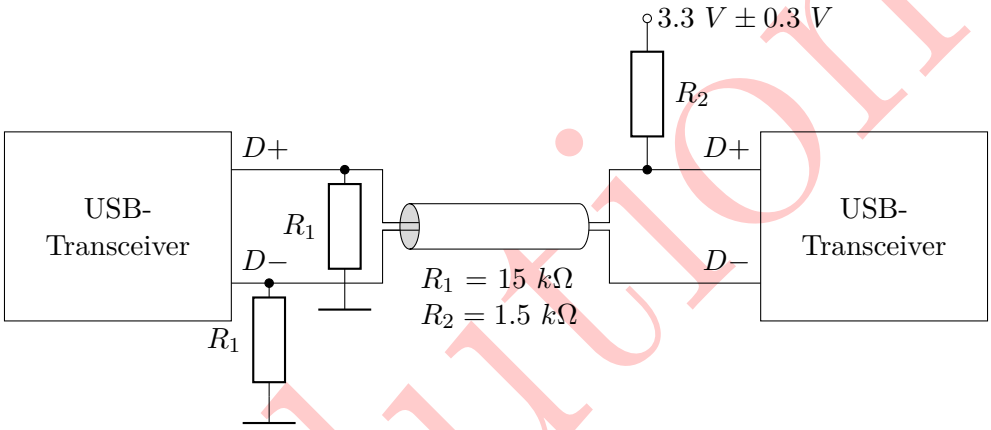
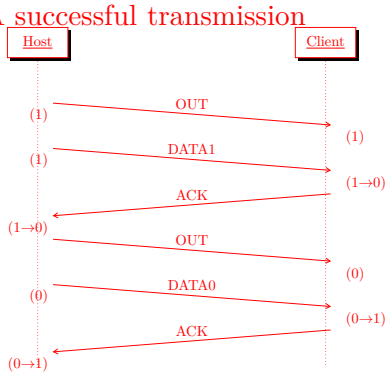


Figure 2.1: Example for resistor configuration at 12Mbit/s

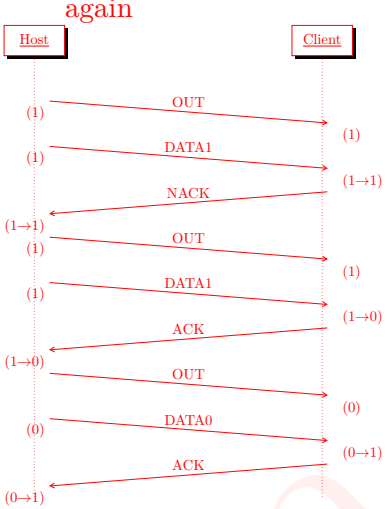
B) To reduce the probability of errors during the handshake phase of a transaction, two data PIDs (DATA0 and DATA1) are used. The data PID is changed after every successful transmission. For that reason the sender and the receiver both have a „data toggle sequence bit“. At the receiver this only changes if correct data with a correct PID has been accepted. At the sender it changes when a valid ACK-Handshake is received. Both participants of a transmission first have to synchronize their bits during the setup phase of a control transfer (see Figure 2.2, the bracketed values correspond to the value of the “data toggle sequence bits”; at X/Y they are still undefined). 1
Starting from the state of 2.2, specify the flow charts for the following cases (always consider a transfer from host to device):

1. A successful transmission
2. A data packet is rejected and only accepted after being transmitted again
3. The handshake packet of a transmission has been mutilated. The data is transmitted again and accepted then

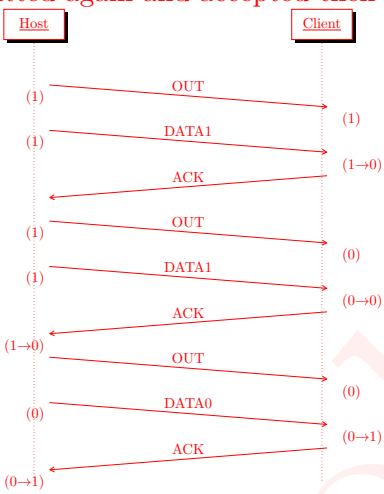
A successful transmission



A data packet is rejected and only accepted after being transmitted again



The handshake packet of a transmission has been mutilated. The data is transmitted again and accepted then



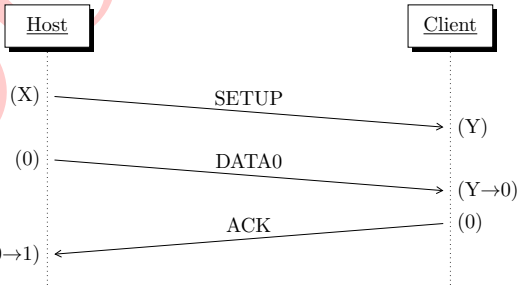


Figure 2.2: Synchronization of the data toggle sequence bits

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Task 3: Flexray: Bus Access

In this task we want to investigate the data transmission and scheduling with Flexray. The used topology is shown in Figure 3.1. Additionally, the slot durations for the scheduling are given in Table 3.1.

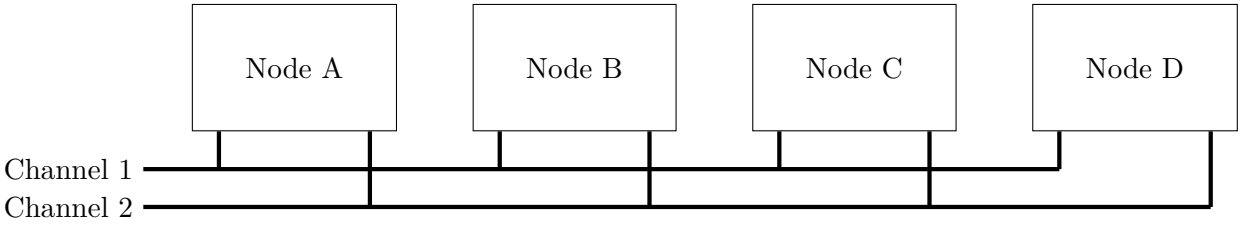

Figure 3.1: Flexray Topology

Static slots	Minislots
$5\mu s$	$100ns$

Table 3.1: Slot durations

A) In Table 3.2 the nodes shown in Figure 3.1 and the assignment of their available frames to the static slots are given. Complete the signal diagram in the Figure 3.2 and perform the static scheduling of the frames according to the Table 3.2.

2

Node	Static Slots	Frames	Redundant Frames
A	1, 3, 5	A1, A2, A3	A2
B	2, 4	B1, B2	B2
C	1, 4	C1, C2	—
D	5	D1	—

Table 3.2: Static Node Assignments

B) Calculate the duration of a complete communication cycle! Assume a Network Idle Time (NIT) of $1\mu s$ and that all minislots depicted in Figure 3.2 are idle!

1

$5 * t_{static} + 10 * t_{dynamic} + t_{NIT} = 5 * 5\mu s + 10 * 0.1\mu s + 1\mu s = 27\mu s$

C) What is the purpose of the minislots with regard to bus access, which are used in the dynamic segment of the communication cycle? Is it possible that multiple nodes can own the same minislot? Justify your answer!

2

Prioritized bus access within the dynamic segment controlled with a slot count. Not possible for multiple nodes to own the same minislot: Similar to static slots each minislot is exclusively owned by one FlexRay node. A minislot thereby only defines a potential start time of a frame transmission in the dynamic segment.

D) In Table 3.3 the parameters for the dynamic segment are given. Complete the signal diagram in the Figure 3.2 and perform the dynamic scheduling of the frames for Channel 1 and Channel 2 according to the Table 3.3. Number the minislots with slot IDs dependent on the length of your scheduled frames. Note that each channel offer its own minislots for transmission.

2

Node	Frames	Slot-ID	Frame Duration
A	A7	7	$100ns$
B	B9	9	$300ns$
C	C8	8	$500ns$
D	D6	6	$400ns$
	D11	11	$200ns$

Table 3.3: Dynamic Segment Parameters

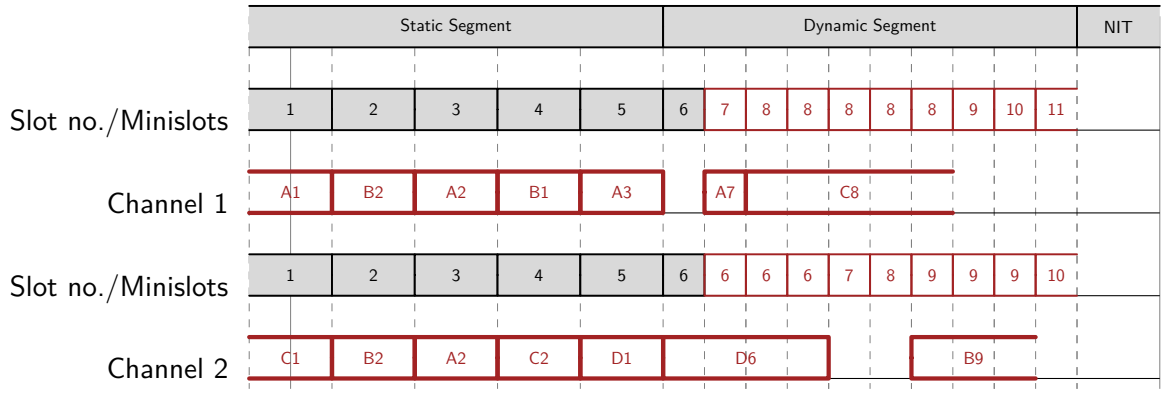

Figure 3.2: Signal sequence